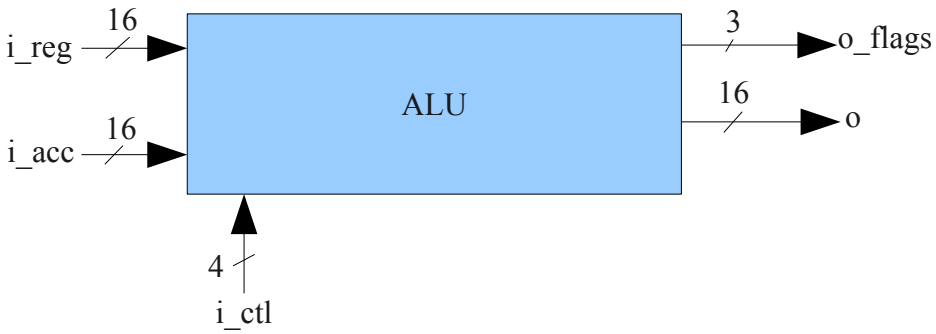
ALU Operation description for the TRAJAN PROCESSOR
ASR1 2008/2009 ENS-Lyon



i_ctl	Description	Output o	Output o_flags
0000	Forward i_reg	O = i_reg;	o_flags[0] = 1 when o=0 o_flags[1] = sign(o); o_flags[2] = add_v_flag when i_ctl = "0001" else sub_v_flag when i_ctl = "0010" else mult_v_flag when i_ctl = "0011" else '0';
0001	Add	o=i_reg+i_acc;	
0010	Sub	o=i_reg-i_acc;	
0011	Mul	o=i_reg(7:0)*i_acc(7:0);	
0100	Swap	o=i_acc(7:0),i_acc(15:8);	
0101	And	o=i_reg AND i_acc;	
0110	Or	o=i_reg OR i_acc;	
0111	Xor	o=i_reg XOR i_acc;	
1000	Not	o=i_reg NOT i_acc;	
1001	LSR	o=i_acc >> i_reg;	
1010	LSL	o=i_acc << i_reg;	
1011	ROR	o=i_acc >>ROTATE>> i_reg;	
1100	ROL	o=i_acc <<ROTATE<< i_reg;	

*Mention:

The multiplication operation multiplies two 2's complement numbers on 8 bits. It is the responsibility of the user to make sure that the operands fit within the interval [-128;127].

The operands are i_reg(7:0) and i_acc(7:0) seen as signed numbers in 2's complement.